AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A random number generating method in an electronic device using~~:~~ a random number, the method comprising:

providing an electronic device including a plurality of unit circuits each having a corresponding noise source, including a first logic circuit and a second logic circuit~~formed into~~, each logic circuit having ~~an identical~~a same shape and each being formed through a same~~an identical~~ fabrication process on a substrate of semiconductor material, and an amplifier circuit to which an output of the corresponding noise source is supplied, the electronic device also including a signal variation detector circuit to which outputs from said plurality of unit circuits are supplied;

causing said plurality of unit circuits and said signal variation detector circuit to perform operations including:~~for forming~~

generating a binary signal at each unit circuit by amplifying ~~a~~ noise superposed on ~~the~~ a differential voltage

of threshold voltages of the first and the second logic circuits of the respective unit circuit; ~~and~~

generating, with~~a~~ said signal variation detecting circuit, ~~for forming~~ an output signal in response to a variation in any of ~~a~~the ~~plurality of~~ binary signals outputted from the ~~plurality of~~ respective unit circuits~~,~~; and

~~wherein~~ combining a plurality of the binary signals outputted from the signal variation detecting circuit ~~are combined~~ to generate a random number.

2. (Currently Amended) The random number generating method as claimed in claim 1,

wherein, in each respective unit circuit, ~~the~~ said first and ~~the~~ second logic circuits ~~and the amplifier circuit~~ are formed ~~by~~ with logic gate circuits each having a first and a second input, respectively,

~~the first input and output of~~ the logic gate circuit ~~corresponding to~~in the first logic circuit ~~are~~ being configured to have its output connected~~,~~ to its first input,

~~the first input of~~ the logic gate circuit ~~corresponding to~~ in the second logic circuit being configured to have its first input connected to~~is connected to the commonly~~

~~connected input and~~ an output of the logic gate circuit ~~corresponding to~~ in the first logic circuit,

wherein the amplifier circuit includes a plurality of logic gate circuits each having a first input and a second input, said plurality of logic gate circuits being connected in series so that~~whose~~ an ~~first~~output ~~input~~of a logic gate circuit ~~and output are~~ is connected ~~vertically~~ to the first input of a next logic gate circuit in the series, and

wherein, when~~the~~ an operation control signal is supplied to the second inputs~~input~~ of the logic gate circuits, respectively~~gate constituting the first logic circuit, the second logic circuit, and the amplifier circuit so as to set the~~ said plurality of ~~units~~ unit circuits are caused ~~to an operation state~~ to generate ~~a~~ the random number via the signal variation detecting circuit.

3. (Currently Amended) The random number generating method as claimed in claim 2,

wherein said electronic device is further provided with an order circuit configured to generate the operation control signal,

wherein the plurality of unit circuits are successively selected in response to ~~an~~ said operation control signal ~~formed~~ generated by ~~an~~ said order circuit and output signals

~~of~~ from all of the unit circuits are outputted serially so as to generate a 1-bit random number by the signal variation detecting circuit.

4. (Currently Amended) The random number generating method as claimed in claim 3,

wherein the signal variation detecting circuit includes~~uses~~ an exclusive logic circuit and is configured to generate the random number by~~for~~ serially receiving output signals ~~serially outputted~~ from the respective unit circuits successively selected correspondingly to the operation control signal supplied by the order circuit ~~and an output signal preceding by one so as to generate the random number~~.

5. (Currently Amended) The random number generating method as claimed in claim 3, further generating an identification signal unique to a semiconductor chip or an integrated circuit on which said unit circuits are formed by a combination of ~~wherein~~the output signals ~~of~~ from all of the unit circuits corresponding to the 1-bit random number ~~is also used as a chip identification signal~~.

6. (Currently Amended) The random number generating method as claimed in claim 1,

wherein said electronic device is further provided with an arithmetical random number generating circuit configured to generate an arithmetical random number,

wherein the random number generating method further comprises:

supplying the random number ~~formed~~ generated by the signal variation detecting circuit ~~is~~ to said arithmetical random number generating circuit; and

causing said arithmetical random number generating circuit to generate the arithmetical random number~~used~~ using the random number supplied from the signal variation detecting circuit as an initial value of the arithmetical random number to be generated by~~a~~ the arithmetical random number generating circuit ~~of the arithmetic method, and~~

~~a random number is generated by the random number generating circuit of the arithmetic method~~.

7. (Currently Amended) A random number generating method in an electronic device using a random number, the method comprising:~~,~~

providing an electronic device including~~wherein a signal of plural bits outputted from~~ a plurality of unit circuits each having a corresponding noise source including a first logic circuit and a second logic circuit, each logic

circuit having a same ~~formed into an identical~~ shape and each being formed through ~~an identical~~ a same fabrication process on a substrate of semiconductor material,and an amplifier circuit to which an output of the corresponding noise source is supplied, the electronic device also including a signal variation detector circuit to which outputs from said plurality of unit circuits are supplied and an arithmetical random number generating circuit configured to generate an arithmetical random number; and

causing said plurality of unit circuits and signal variation detector circuit to perform operations including:

generating~~for forming~~ a binary signal at each unit circuit by amplifying noise~~a noise~~ superposed on ~~the~~ a differential voltage of threshold voltages of the first and the second logic circuits of each respective unit circuit;

generating, at said signal variation detecting circuit, an output signal in response to a variation in any of the binary signals outputted from the respective unit circuits; and

combining a plurality of the binary signals outputted from the signal variation detecting circuit to generate a random number;

supplying the random number generated by the signal variation detecting circuit to said arithmetical random number generating circuit; and

causing said arithmetical random number generating circuit to generate the arithmetical random number using the random number supplied from the signal variation detecting circuits ~~is transferred~~ as an initial value of the arithmetical random number to be generated by~~to a~~ the arithmetical random number generating circuit ~~of the arithmetic method; and~~

~~a random number is generated from the random number generating circuit of the arithmetic method~~.

8. (Currently Amended) A semiconductor integrated circuit device comprising: a plurality of unit circuits each having a first and a second logic circuit formed into an identical shape through an identical fabrication process and an amplifier circuit for forming a binary signal by amplifying a noise superposed on the differential voltage of threshold voltages of the first and the second logic circuits; and

a signal variation detecting circuit for forming an output signal in response to a variation in any of a plurality of binary signals outputted from the plurality of unit circuits,

wherein a random number is generated from a binary signal outputted from the signal variation detecting circuit.

9. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 16~~8~~,

wherein the first and ~~the~~ second logic circuits, of each respective unit circuit,~~circuit and the amplifier circuit~~ are formed ~~by~~ with logic gate circuits each having a first and a second input, respectively,

~~the first input and output of~~ the logic gate circuit ~~corresponding to~~in the first logic circuit being configured to have its outputare connected to its first input,

the ~~first input of the~~ logic gate circuit ~~corresponding to~~ in the second logic circuit being configured to have its first input~~is~~ connected to ~~the~~an ~~commonly connected input and~~ output of the logic gate circuit ~~corresponding to~~ in the first logic circuit,

wherein the amplifier circuit includes a plurality of logic gate circuits each having first and second inputs, said plurality of logic gate circuits being connected in series so that an output of a logic gate circuit is connected to the first input of a next logic gate circuit in the series,

wherein, when an operation control signal is supplied to the second input of the logic gate circuits, respectively, said plurality of unit circuits are caused to generate a random number via the signal variation detecting circuitcircuit corresponding to the first and the second logic circuit,

the amplifier circuit includes a plurality of logic gate circuits whose first input and output are connected vertically, and the operation control signal is supplied to the second input.

10. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 9,

further comprising an order control circuit configured to generate the operation control signal,

wherein the plurality of unit circuits are successively selected in response to ansaid operation control signal formed generated by an the order control circuit, and

wherein the signal variation detecting circuit is arranged at the an output unit one of the plurality of unit circuits.

11. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 910, wherein the signal

variation detecting circuit includes an exclusive logic circuit configured to generate the random number by~~for~~ serially receiving output signals ~~outputted~~ from the respective unit circuits successively selected corresponding to the operation control supplied by the order control circuit ~~so as to generate the random number~~.

12. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 11, wherein the logic gate circuits of each unit circuit are logic gate circuits of CMOS configuration and when the unit circuits are set to a non-active state by the operation control signal, a P-channel MOSFET of the logic gate circuit of ~~the next stage~~ each respective second logic circuit is set to an OFF state.

13. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 11, wherein

the plurality of unit circuits are arranged in a matrix,

wherein each ~~of the~~ unit ~~circuits~~ circuit arranged in the matrix is provided with~~has~~ an input unit ~~having~~ configured with a logic gate circuit having a first input and a second input,

wherein, in response to a row and a column ~~selecting~~ selection signal ~~are~~ supplied to the first input and the second input, said input unit is configured to output ~~so that the output forms an~~ the operation control signal which causes ~~for setting~~ the logic gate circuits ~~circuit constituting~~ in the first logic circuit and the second logic circuit to be in a selected state,

wherein said matrix is configured so that the second input of the logic gate circuit of the amplifier in one of the unit of the circuits is supplied with an output signal of ~~a~~ another of the unit circuits which is arranged at ~~circuit of~~ a stage preceding ~~stage arranged~~ in ~~the~~ a row direction of the matrix ~~is transmitted to the second input of the logic gate circuit constituting the amplifier circuit of each unit circuit and~~ such that when the operation control signal is in a non-selected state, the amplifier circuit in said one of the unit circuits amplifies the output signal from ~~of~~ said another of the unit circuits of the preceding stage.

14. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 12 ~~11~~, wherein

each ~~the~~ MOSFET in ~~MOSFET constituting~~ ~~the~~ a respective unit circuit ~~circuit~~ has a gate length and a gate width

formed greater than ~~a gate length and a gate width~~ that of ~~the~~ MOSFETs in ~~MOSFET constituting the other~~ logic circuits ~~containing~~ of the signal variation detecting circuit or the order control circuit.

15. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 11, wherein

the order control circuit includes a test mode configured to determine similar~~for selecting the same~~ unit circuits a plurality of times continuously,

wherein the semiconductor integrated circuit device is further provided with a circuit ~~is provided~~ for counting ~~the~~ a number of unit circuits forming different outputs among the output signals outputted a plurality of times from the same unit circuit, and when the number of unit circuits forming the different output signals is one or more, the random number generating circuit is judged to have a high quality.

16. (New) A semiconductor integrated circuit device formed with a random number generating member configured to supply a random number to an application specific function of the semiconductor integrated circuit device, said random number generating member comprising:

a plurality of unit circuits each having a corresponding noise source including a first logic circuit and a second logic circuit, each logic circuit having a same configuration and each being formed through a same fabrication process on a substrate of semiconductor material, and an amplifier circuit to which an output of the corresponding noise source is supplied; and

a signal variation detecting circuit to which outputs from said plurality of unit circuits are supplied;

wherein said plurality of unit circuits and said signal variation detector circuits are configured to perform operations including:

generating a binary signal at each unit circuit by amplifying noise superposed on a differential of a threshold voltage of the first logic circuit and second logic circuit of each respective unit circuit;

generating, at said signal variation detecting circuit, an output signal in response to a variation in any of the binary signals outputted from the respective unit circuits;

combining a plurality of the binary signals outputted from the signal variation detecting circuit to generate a random number; and

supplying the generated random number to the application specific function of the semiconductor circuit device.

17. (New) An electronic device formed with a random number generating member configured to supply a random number to an application specific function of the electronic device, said random number generating member comprising:

a plurality of unit circuits each having a noise source including a first logic circuit and a second logic circuit, each logic circuit having a same configuration and each being formed through a same fabrication process on a substrate of semiconductor material, and an amplifier circuit to which an output of the corresponding noise source is supplied; and

a signal variation detecting circuit to which outputs from said plurality of unit circuits are supplied;

wherein said random number generating member is configured to perform operations including:

generating a binary signal at each unit circuit by amplifying noise superposed on a differential of a threshold voltage of the first and the second logic circuits of the respective unit circuit;

generating, at said signal variation detecting circuit, an output signal in response to variation in any of the binary signals outputted from the respective unit circuits;

combining a plurality of the binary signals outputted from the signal variation detecting circuit to generate a random number; and

supplying the generated random number to the application specified function of the electronic device.

18. (New) A random number generating method in an electronic device, the method comprising:

providing a random number generation member including a plurality of unit circuits each having a corresponding noise source including a first logic circuit and a second logic circuit, each logic circuit having a same configuration and being formed through a same fabrication process on a substrate of semiconductor material, and an amplifier circuit to which an output of the corresponding noise source is supplied, the random number generation member also including a signal variation detector circuit to which outputs from said plurality of unit circuits are supplied;

mounting the random number generation member to the electronic device; and

causing said random number generation member to perform operations including:

generating a binary signal at each unit circuit by amplifying noise superposed on a differential of threshold voltages of the first and the second logic circuits of each respective unit circuit;

generating, at said signal variation detecting circuit, an output signal in response to a variation in any of the binary signals outputted from the respective unit circuits;

combining a plurality of the binary signals outputted from the signal variation detecting circuit to generate a random number; and

supplying the generated random number to an application specific function of the electronic device.